WHAT IS CLAIMED IS:

1. A power supply system comprising:

a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay; and

a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal.

2. The power supply system of claim 1 and further comprising a digital-to-analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals.

3. The power supply system of claim 2 wherein the DAC includes:

a decoder that converts the plurality of latched signals to a plurality of edge words;

an integrator that averages a number of edge words to generate a plurality of control signals;

a plurality of control circuits connected to the power node, each control circuit receiving a control signal;

a plurality of resistor nodes, each resistor node being connected to a control circuit; and

a plurality of resistors connected to the plurality of resistor nodes such that each resistor is connected to a resistor node.

4. The power supply system of claim 3 wherein the decoder includes an exclusive OR gate.

5. The power supply system of claim 4 wherein the exclusive OR gate is free of a transmission gate.

6. The power supply system of claim 2 wherein the plurality of resistors are connected in series.

7. The power supply system of claim 6 wherein the resistors are connected between a power supply voltage and ground.

8. The power supply of claim 2 wherein the propagation delay detector includes a plurality of substantially equal delay blocks that have a corresponding plurality of outputs that output the plurality of detection signals as a thermometer code.

9. The power supply of claim 2 wherein the sample signal is a quadrature signal with respect to the launch signal, and the launch signal is a clock signal.

10. The power supply system of claim 2 and further comprising a reset circuit that generates a reset signal in response to the launch signal and the sample signal.

11. The power supply system of claim 10 wherein a rising edge of the sample signal precedes a rising edge of the launch signal.

12. The power supply of claim 10 wherein the power node is connected to the latch circuit and the reset circuit.

13. The power supply of claim 8 wherein the plurality of delay blocks and the plurality of detection signals are unequal.

14. The power supply system of claim 2 and further comprising a current boosting stage connected to the DAC.

15. The power supply system of claim 9 wherein the latch circuit outputs the plurality of latched signals as a thermometer code.

16. A power supply system comprising:

a plurality of power supply circuits, each power supply circuit having:

a propagation delay detector that measures a propagation delay of a launch signal, and outputs a plurality of detection signals that identify the propagation delay;

a latch circuit that latches the detection signals as a plurality of latched signals in response to a sample signal; and

a digital-to-analog converter (DAC) connected to the latch, the DAC receiving the plurality of latched signals, and generating a voltage on a power node in response to the plurality of latched signals; and

a plurality of current boosting stages, each power supply circuit being connected to a current boosting stage.

17. The power supply system of claim 16 wherein the plurality of power supply circuits are formed on a first chip, and the plurality of current boosting stages are formed on a second chip.

18. The power supply system of claim 17 wherein the current boosting stages are operational amplifiers.

19. A method of providing power, the method comprising the steps of:

measuring a propagation delay of a launch signal with a propagation delay detector, and outputting a plurality of detection signals that identify the propagation delay;

latching the detection signals in response to a sample signal to form a plurality of latched signals; and

generating a voltage in response to the plurality of latched signals, and outputting the voltage to the propagation delay detector.

20. The method of claim 19 wherein the sample signal is a quadrature signal with respect to the launch signal.

21. The method of claim 19 wherein the generating step includes the step of converting the plurality of latched signals to a plurality of control signals, the control signals having first logic states and second logic states, and only one of the control signals having a first logic state at a time.